Preliminary Program

Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors

29 July - 3 August 2007

Il Ciocco Hotel and Conference Center, Barga, Italy

Conference Chair
Dr. Yue Kuo
Texas A&M University

Conference Co-Chairs
Prof. Michael Shur
Rensselaer Polytechnic Institute
Dr. Dieter Ast
Cornell University

ECI
Engineering Conferences International
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Sunday, July 29, 2007

16:30 - 18:30 Registration
18:30 - 20:00 Opening Reception
20:00 - 21:30 Opening Dinner

Monday, July 30, 2007

07:30 - 08:30 Breakfast Buffet
08:30 - 08:45 Welcome and Conference Overview
   Y. Kuo, D.G. Ast, and M. Shur
   ECI Technical Liaison N. Li
08:45 - 09:30 Nanotechnology for the Post-CMOS Scaling ERA
   T.C. Chen, IBM
09:30 - 10:15 Low-Temperature Polysilicon History and a CPU with an Operating Frequency in the GHZ Range
   S. Yamazaki, SEL
10:15 - 10:45 Coffee Break
10:45 - 12:30 Challenges in Scaling and Devices
   Session Chairs: M. Shur, Rensselaer Polytechnic University
   S. Hamaguchi, Osaka University, Japan
10:45 - 11:10 Performance Limitations of Si Bulk CMOS And Alternatives for Future ULSI
   K.C. Saraswat, Stanford University
11:10 - 11:35 Electrical Performance and Reliability Aspects of Strain Engineered Deep Submicron CMOS Technologies
   C. Claeys, IMEC
11:35 - 12:00 Technology Trend and Application of TFT-LCDs
   Y. Yamamoto, Sharp
12:00 - 12:25 The Small Differences Between 45nm and 45 Inches
   C. Reita, CEA-LETI
12:25 - 12:30 Questions/Announcements
12:30 - 14:00 Lunch
14:00 - 17:00 Free Time for leisure, recreation, discussion, ad hoc sessions
17:00 - 17:30 Afternoon Coffee
17:30 – 19:30  Challenges in Devices, Scaling, etc.
Session Chairs: K. Saraswat, D. Buckley

17:30 – 17:55  Device Performance and Reliability of Fully Depleted SOI Transistors Low-Temperature Poly-Si TFTs
M. Hatano, M. Matsumura, M. Tai, Y. Toyota, M. Ohkura, Hitachi

17:55 – 18:20  TFT Technologies for Large Area Electronics
J. Jang, Kyung Hee University

18:20 – 18:45  Nanoscale Large Area Electronics - Device and Material Integration Challenges
A. Nathan, University College London

18:45 – 19:10  ULSI vs. TFT - What can they learn from each other?
Y. Kuo, Texas A&M University

19:10 – 19:30  Discussion

20:00 – 21:30  Dinner

21:30 – 22:30  Social Hour
Tuesday, July 31, 2007

07:30 - 08:30  Breakfast Buffet

08:30 - 10:35  Challenges in Dielectrics and Semiconductors in ULSIC
Session Chairs:  R. Street, PARC
               J. Jang, KyungHee University

08:30 - 08:55  Electrical Characterization of Advanced Gate Dielectrics for Scaled CMOS Technology
T.P. Ma, Yale University

08:55 - 09:20  Nano-Length Scales for Coherent D-State PI-Bonding: A New Approach to Electron and Hole Asymmetric Trapping in HfO\textsubscript{2} Gate Dielectrics, and Defects at LAALO\textsubscript{3}-SRTIO\textsubscript{3} Hetero-Junction Transition Metal(TM) Rare Earth (RE) Atom Oxide Interfaces
G. Lucovsky, North Carolina State University

09:20 - 09:45  Scanning Transmission Electron Microscopy of High-K Gate Stacks for Silicon CMOS
S. Stemmer, UCSB

09:45 - 10:10  HfO\textsubscript{2} as a Gate Dielectric for Future CMOS Technology
E. Cartier, B. P. Linder, V. K. Paruchuri, V. Narayanan, IBM SRDC

10:10 - 10:40  Coffee Break

10:40 - 12:30  Challenges in Dielectrics and Semiconductors in TFTs
Session Chairs:  A. Nathan, University College London
                G. Lucovsky, North Carolina State University

10:40 - 11:05  Polymer Semiconductors for Displays and Image Sensors
R. Street, M. Chabinyc, J. Northrup, PARC

11:05 - 11:30  Improvement of Silicon Based Thin Film Transistors Performances by Modifying Technological Fabrication Process Steps: A Similar Approach with ULSI Technology
O. Bonnaud, T. Mohammed- Brahim, University of Rennes 1

11:30 - 11:55  Grain Boundary Characterization in Sequentially Laterally Solidified Polycrystalline-Silicon Thin Film Transistors
A. Valletta, A. Bonfiglietti, M. Rapisarda, L. Mariucci, A. Pecora,
G. Fortunato, S.D. Brotherton, IFN - CNR

11:55 - 12:10  Transparent OTFTS with Color Filtering Functional Gate Insulators
C.-S. Chuang, F.-C. Chen, H.-P.D. Shieh, NCTU

12:10 - 12:25  Verase Improvement for Split-Gate Embedded Flash Through Poly Grain Size Reduction
H.S. Ng, H.M Tan, X-FAB

12:25 - 12:30  Discussion
12:30 - 14:00  Lunch
14:00 - 17:00  Free Time for leisure, recreation, discussion, ad hoc sessions
17:00 - 17:30  Afternoon Coffee
17:30 - 20:00  **Challenges In Dielectrics and Semiconductors in General**
   Session Chairs:  T.P. Ma, Yale University
   O. Bonnaud, University of Rennes 1

17:30 - 17:45  **Defects and Defect Precursor Reductions in Non-Crystalline Thin Films: Intermediate States Generated by Chemical Bonding Self-Organizations Which Include Broken Bond-Bending Constraints**

17:45 - 18:00  **Electron Spin Resonance Studies of Silicon Nano-Crystal Flash Memory Devices**
   J.T. Ryan, P.M. Lenahan, L. Visnubhotla, S. Straub, M. Ramachandran, R. Rao, T. Merchant, Pennsylvania State University

18:00 - 18:15  **Improved Electrical Characteristics of MOS Devices With Ultrathin Gate Oxide Grown by Chemical Oxidation**
   N. DasGupta, B.J. Kailath, A. DasGupta, Indian Institute of Technology, Madras

18:15 - 18:30  **Improved Electrical Properties of NILC-TFT Using Simple Gettering Methods**
   Y.C.S. Wu, C.-C Lin, C.-M. Hu, P.H. Hsiao, NCTU

18:30 - 20:00  **Panel Discussion: Challenges in Devices, Materials, and Applications**
   Moderators:  S. Uchikoga, Toshiba, Japan
   C. Claeys, IMEC, Belgium

20:15 - 21:45  Dinner
21:45 - 22:45  Social Hour
Wednesday, August 1, 2007

07:30 - 08:30 Breakfast Buffet

08:30 - 10:35 Challenges in Interconnects, Contacts, and Defect Inspections
Session Chairs: D. Ast, Cornell University
G. Bersuker, Sematech

08:30 - 08:55 Air Cavity Generation for Interconnect and High Resolution Displays
P.A. Kohl, Georgia Tech

08:55 - 09:20 Low and UltraLow-K Dielectrics for High Performance Interconnects
A. Grill, V. Patel, S. Gates, S. Nguyen, C. Dimitrakopoulos, D. Restaino, IBM

09:20 - 09:45 AFM Observation of Nanostructure and Morphology of Electrodeposited Copper Metallization during Room-Temperature Aging
D.N. Buckley, S. Ahmed, T.T. Ahmed, S. Nakahara, University of Limerick

09:45 - 10:10 In-Line Automatic Defect Inspection and Repair Method for A High Yield TFT Array Production

10:10 - 10:25 Heterojunction between Silicon and Semiconducting Metal Silicides
M. Baleva, N. Todorov, M. Marinova, Aleksander

10:25 - 10:55 Coffee Break

10:55 - 12:40 Challenges in Modeling, Theories, etc.
Session Chairs: P. Kohl, Georgia Tech
A. Grill, IBM

10:55 - 11:20 Modeling of Thin Film Transistors with Non-Ideal Contacts
M.S. Shur, D. Veksler, A. Kudymov, B. Iñiguez, W. Jackson, RPI

A. Baiano, R. Ishihara, N. Karaki, S. Inoue, W. Metselaar, K. Beernakker

11:35 - 12:00 Fast and Slow Parameter Instability Processes in High-K Gate Stack Devices
G. Bersuker, SEMATECH

12:00 - 12:25 Atomic-Scale Analyses of Non-Equilibrium Surface Reactions During Plasma Processing
S. Hamaguchi, Osaka University
12:25 – 12:50 Controlling the Nucleation Site and Crystal Orientation During Excimer-Laser Annealing Processes In Thin Amorphous Si Films on Glass: A Molecular-Dynamic Study
T. Motooka, Kyushu University

12:50 – 14:00 Lunch

14:00 – 18:30 Free Time for leisure, recreation, discussion ad hoc sessions
Optional Excursion to Lucca

18:30 – 20:00 Poster session (with wine)
Session Chairs: K. S. Karim, Simon Fraser University
T. Serikawa, Osaka University

Molecular Dynamics Simulations FOR Reactive Ion Etching of SiO$_2$ and Si COH Dielectric Films
T. Takizawa, S. Hamaguchi, Osaka University

Study of Structure and Electrical Characteristics of Silicon Oxynitride LayersSynthesized by Dual Ion Implantation in Silicon and Their Annealing Behavior
A. D. Yadav, G. Bhatt, S. K. Dubey, University of Mumbai

Bathtub-Shaped Hazard Rate Function for Ultra-Thin Gate Dielectrics
T. Yuan and W. Kuo, University of Tennessee

Leakage Current-Free Pixel Structure Using a Blocking Transistor for Active-Matrix Display
H.-S. Park and M.-K. Han, SNU

Performance Improvement of Organic Thin-Film Transistors by Ammonia Plasma Pretreatment on the Surface of Gate Dielectric
C.-L. Fan, T.-H. Yang, C.-H. Huang, C.-I. Lin, NTUST

Radiation Damages to a-Si: H TFTS Induced From Fabrication Process and Environment
Y. Kuo, H. Nominanda, C.-C. Chen, C.-C. Hwang, TAMU

Investigation of Hump Degradation by F-N Stress for Narrow Width N-MOSFETS with Shallow Trench Isolation (STI)
J. Y. Seo, Samsung

SiO$_2$/ SiC Interface Electrical Characteristics
H. Boudinov, Rodrigo Palmieri, Claudio Radtke, UFRGS

The Hysteresis Phenomenon In A-Si: H TFT and POLY-Si TFT in AMOLED

Low Hysteresis Characteristics of Pentacene Thin-Film Transistor and Inverter
Surface-Treatment Effects on Organic Thin-Film Transistors by Atmospheric-Pressure Plasma Technology
K. M. Chang, C. H. Lin, S. X. Huang, NCTU

Transistor and Circuit Operation of Complimentary Organic Thin Film Devices

Organic Logic-Circuits Using Screen Printing Method

An Approach to Calculate and Plot V-I Characteristics for 4H-SiC Schottky Barrier Diode for Different Contact Metals Using Iteration Method and C++ Programming
R. Talwar and A.K. Chatterji, RIMT

20:00 – 22:00 Dinner

22:00 – 23:00 Poster Session (continued) and Social Hour
Thursday, August 2, 2007

07:30 - 08:30  Breakfast Buffet

08:30 - 10:35  Challenges in Processes and Reliability
Session Chairs:  W. Tonti, IBM
                W. Milne, Cambridge University

08:30 - 08:55  Demonstration of High Performance Low Temperature Crystalline Silicon (LTCS) Thin-Film Transistors
C.K. Williams, J. Cites, Corning

08:55 - 09:20  New LC Method for GHZ Level TFT Operation
K. Tanaka, T. Omata, T. Moriwaka, H. Oishi, S. Yamazaki, SEL

09:20 - 09:45  Reliability of Short Channel Polycrystalline Silicon Thin Film Transistor on the Glass Substrate
M.-K. Han, SNU

09:45 - 10:10  Moisture Induced Accelerated Aging of an Amorphous Silicon TFT-Photodiode Array
W. A. Hennessy, GE

10:10 - 10:25  Physics-Based Percolation Model of Oxide Breakdown
J. Suñé, E. Wu, S. Tous, U. Autònoma Barcelona

10:25 - 10:55  Coffee Break

10:55 - 12:35  Challenges in Reliability
Session Chairs:  M. Hatano, Hitachi
                D. Dawson-Elli, Corning

10:55 - 11:20  MOS Technology Drivers
W. R. Tonti, IBM

11:20 - 11:45  Electromigration Reliability Assessment of Cu-Based Metallization Systems by a Wafer-Level Approach
M. Impronta, A. Marras, I. De Munari, A. Scorzoni, CNR-IMM

11:45 - 12:10  Dielectric Reliability for Future Logic and Non-Volatile Memory Applications: A Statistical Simulation Analysis Approach
P. Pavan, L. Larcher, A. Padovani, U. Modena e Reggio Emilia

12:10 - 12:35  Electron Spin Resonance and Reliability Defects
P.M. Lenahan, Pennsylvania State University

12:35 - 14:00  Lunch

14:00 - 16:00  Free Time for leisure, recreation, discussion ad hoc sessions

16:00 - 16:30  Afternoon Coffee
16:30 – 17:30  **Challenges in fabrication and Defects**  
Session Chairs:  
T. Motooka, Kyushu University  
H.-P. Shieh, National Chiao Tung University

16:30 – 16:45  **High Quality Polycrystalline SI Thin Film Transistors with Sputter-Deposited Very-Thin Gate SiO₂ Films**  
T. Serikawa, M. Miyashita, Y. Uraoka, T. Fuyuki, Osaka University

16:45 – 17:00  **Fabrication of the High Resolution Poly-SI TFTS Array on 3 Inch Glass Substrate Using Ni-Induced Field Aided Lateral Crystallization**  
H.-C Kim, Y.-B. Kim, D.-K. Choi, Hanyang University

17:00 – 17:15  **Magnetic Resonance Studies of Reliability Defects in HFO₂ Based MOS Devices**  
C. Cochrane, J.T. Ryan, P.M. Lenahan, G. Bersuker, Pennsylvania State University

17:15 – 17:30  **High Performance Flexible Organic Thin Film Transistors**  
Y. Seol, N.-E. Lee, S.H. Park, J.Y. Bae, S.S. Lee, J.H. Ahn  
Sungkyunkwan University

17:30 – 19:00  **Panel Discussion: Challenges in Large-Area Fabrication Processes**  
Moderators:  
D.G. Ast, Cornell University  
Y. Yamamoto, Sharp

Panelists:  
A. Nathan, R. Street, W. Tonti, S. Uchikoga,  
Y. Yamamoto, J. Jang, P. Kohl, H.-P. Shieh,  
C. Reita, T.C. Chen, A. Grill, H. Honoki,  
D. Dawson-Ellis, W.B. Jackson, W. I. Milne

20:00  **Conference Banquet**
### Challenges in Nano Structures and Fabrications

**Session Chairs:**
- P. Lenahan, Pennsylvania State University
- M. K. Han, Seoul National University

#### 08:30 – 09:50
- **Carbon Nanotubes and Their Potential Use in Electronic Devices and Circuits**
  - W.I. Milne, Cambridge University

#### 08:55 – 09:20
- **Large Area Flexible Electronics Fabricated Using Imprint Lithography**

#### 09:20 – 09:35
- **Novel Polysilicon Thin-Film Transistors with Nanowire Channel**

#### 09:35 – 09:50
- **Silicon Nanowire Schottky Barrier NMOS Transistors**
  - E. J. Tan, K. L. Pey, G. Cui, N. Singh, G.-Q. Lo, D. Chi, P. S. Lee, Nanyang TU,

### Challenges in Applications and Substrates

**Session Chairs:**
- W.B. Jackson, HP
- M. Shur, RPI

#### 10:20 – 12:05
- **Poly-Si TFT Fabrication on “Non-Display” Glass Substrates**
  - D. G. Ast, Cornell University

#### 10:45 - 11:10
- **CPU for HF and UHF Operation on the Glass and Flexible Substrates**

#### 11:10 – 11:35
- **Intelligent Pixel Architectures for Digital Medical Imaging Applications**
  - K. S. Karim, Simon Fraser University

#### 11:35 – 11:50
- **INGAN Nanostructured Materials: Controlled Synthesis, Characterizations, and Applications**

#### 11:50 – 12:05
- **ZnO and Its Nanostructures for Novel Devices**
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